Support for the amendment of claim 1 is found in the original claim 1 and in the specification on page 8, lines 12 through 22 (which discusses the width c of the bottom surface, the width d of the top surface, and the height p of the conductor pattern), and on page 8, line 30 through page 9, line 5 (which discusses the height p of the conductor pattern and the height h of the lower/protected portion of the conductor pattern).

Support for the amendment of claim 2 is found in the original claims 1 and 2, Figure 1, and the specification on page 7, lines 14 through 25 (which discusses the pattern extending perpendicular to the plane of the drawing).

Support for the amendment of claim 4 is found in the original claims 1 and 4, in Figure 1, and in the specification on page 3, line 31 through page 4, line 2 (which defines lower side surfaces), and page 10, lines 1 through 17 (which discusses the relationship between the height h of the lower portion 31 or side surface 315, versus the height p of the conductor pattern 3).

Support for the amendment of claim 7 is found in the original claims 1 and 7 and in the specification on page 10, line 23 through page 11, line 9 (which discusses how the value X is determined).

Claims 1 and 8 have been further amended to identify the substrate as an "insulative substrate," support for which is found in the specification on page 7, lines 13 through 17.

Objection to Specification

The Examiner has objected to the disclosure because of the following cited informalities:

On page 2, line 14, of the specification "4" should be --94--.

On page 13, line 23, "the" should be --an--.

On page 14, line 15, "41" should be --42--.

Appropriate correction is required.

The present amendment corrects the above informalities. Although page 13, line 23 has two occurrences of the word "the," it is assumed that the first instance of "the" is the one that needs to be corrected. On page 14, line 15, it is assumed that the Examiner meant that "41" should be "42."

Rejection of Claims Under 35 U.S.C. § 112

The Examiner has rejected claims 1 through 7 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner stated:

> In claim 1, the recitations "the width of the bottom surface" and "the width of the top surface" lack proper antecedent basis.
>
> In claim 2, the recitation "the longitudinal direction" lacks proper antecedent basis.
>
> In claim 4, the recitations "the height of he portion," "the portion," and "the height of the conductor pattern" lack proper antecedent basis.
>
> In claim 5, "plating" should be --plate--.
>
> In general, claim 7 is wordy and confusing: in claim 7, it can not be determined what the applicant regards as "a value obtained by dividing one half of a value obtained by subtracting the width of the top surface from the

width of the bottom surface by the height of the conductor pattern is in the range of 0.1 to 2.5.

The present amendment corrects the above informalities, except that the Applicants respectfully traverse the rejection of claim 5 for using the word "plating" instead of the word "plate." The specification specifically uses the word "plating" as both a noun and as a verb, with the grammatical use thereof being readily discernable in context of the rest of the specification. The specification does not use the word "plate," so the suggested amendment would be improper, since the specification would not support such a change.

Rejection of Claims Under 35 U.S.C. § 102

The Examiner has rejected claims 1, 4, 5 and 8 under 35 U.S.C. §102(b), as being anticipated by Shingai et al. (U.S. Patent number 5,886,877). The Examiner stated:

> Note Fig. 7 of Shingai et al., where he/she shows a printed circuit board comprising: a substrate (2a); a conductor pattern (3) formed on the substrate (see Fig. 7); and a protection film (1a) coating the substrate and the conductor pattern (see Fig. 7), wherein the conductor pattern (3) includes a bottom surface contacting the substrate, a top surface opposite to the bottom surface, and a pair of side surfaces, each of the side surfaces having a lower side surface covered by the protection film and an upper side surface exposed from the protection film, and the width of the bottom surface being greater than the width of the top surface (see Fig. 7).

Regarding claim 4, Shingai et al. discloses the height of the portion coated by the protection film (1a) in the conductor pattern (3) is 50% or greater and less than 100% of the height of the conductor pattern (see Fig. 7).

Regarding claim 5, Shingai et al. disclosed the top surfaces and the upper side surfaces being coated by a plate (3a and see Fig. 7).

Regarding claim 8, the method steps are disclosed by Shingai et al. for the same reasons provided for the device claim 1.

The Applicants respectfully submit that the "substrate (2a)" of the Shingai et al. reference differs dramatically from the "substrate" of the present invention. The Shingai et al. reference consistently identifies element (2a) as a "conductor circuit," while there is no indication in the present specification that the substrate would be conductive. On the contrary, the term "substrate 2" is identified in the present specification as being an "insulative substrate" (see page 7, lines 14-15). This distinction, that the substrate is insulative, has been incorporated into the claims by the present amendment.

The present invention has, as an object, providing a printed circuit board and its manufacturing method that provides strong adhesion between an insulative substrate and a conductor pattern and prevents damage of the insulative substrate. The adhesion between the insulative substrate and the conductor pattern is a problem because of the dissimilarities in the nature between the substrate and the conductor pattern. No such dissimilarities exist between the conductor circuit 2a and the bumps 3 of the Shingai et al. reference, because they are both conductive materials.

Notice that the conductor pattern (3), which is cited by the Examiner as including "a bottom surface contacting the substrate, a top surface opposite to the bottom surface, and a pair or side surfaces, each of the side surfaces having a lower side surface covered by the protection film and an upper side surface exposed from the protection film, and the width of the bottom surface being greater than the width of the top surface" actually contacts a conductor circuit instead of an insulative substrate.

The Applicants respectfully request that the Examiner clarify his comments regarding claim 8. The Patent Rules [37 C.F.R. § 1.104(c)(2)] state that "The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified." Since claim 8 is a method claim, with an etching step, an application of an insulative protection film, and a removal of part of that protection film, and since the "reasons provided above" do not mention any such steps, the Examiner's basis for the rejection is unclear.

Regarding claim 8, it must be pointed out that the conductor pattern (which is formed so that a width of a bottom surface contacting the substrate is greater than a width of a top surface, which is opposite the bottom surface) is etched on an insulative substrate. There isn't any such a conductor pattern on an insulative substrate disclosed in the Shingai et al. reference.

Based upon the present amendment and the comments above, Applicants respectfully request that the Examiner withdraw his rejection to claims 1, 4, 5 and 8.

The Examiner also rejected claims 1 and 8 under 35 U.S.C. §102(b), as being anticipated by Kimiya (Publication number 01238132). The Examiner stated:

Note Fig. 2 of Kimiya, where he/she shows a printed circuit board comprising: a substrate (36); a conductor pattern (42) formed on the substrate (see Fig. 2); and a protection film (38) coating the substrate and the conductor pattern (see Fig. 2), wherein the conductor pattern (42) includes a bottom surface contacting the substrate, a top surface opposite to the bottom surface, and a pair of side surfaces, each of the side surfaces having a lower side surface covered by the protection film and an upper side surface exposed from the protection film, and the width of the bottom surface being greater than the width of the top surface (see Fig. 2).

Regarding claim 8, the method steps are disclosed by Kimiya for the same reasons provided above for the device claim 1.

The Applicants respectfully submit that the "substrate (36)" of the Kimiya reference differs dramatically from the "substrate" of the present invention. The abstract of the reference identifies element (36) as an "Au conductor layer," while there is no indication in the present specification that the substrate itself would be conductive. On the contrary, the term "substrate 2" is identified in the specification as being an "insulative substrate" (see page 7, lines 14-15). This distinction, that the substrate is insulative, has been incorporated into the claims by the present amendment.

As stated above, the present invention has, as an object, providing a printed circuit board and its manufacturing method that provides strong adhesion between an insulative substrate and a conductor pattern and prevents damage of the insulative substrate. The adhesion between the insulative substrate and the conductor pattern is a problem because of the dissimilarities in the

nature between the substrate and the conductor pattern. No such dissimilarities exist between the Au conductor layer 36 and the Ni-containing layers 42 of the Kimiya reference, because they are both conductive materials.

Notice that the conductor pattern (42), which is cited by the Examiner as including "a bottom surface contacting the substrate, a top surface opposite to the bottom surface, and a pair of side surfaces, each of the side surfaces having a lower side surface covered by the protection film and an upper side surface exposed from the protection film, and the width of the bottom surface being greater than the width of the top surface" actually contacts a conductor circuit instead of an insulative substrate.

The Applicants respectfully request that the Examiner clarify his comments regarding claim 8. Since claim 8 is a method claim, with an etching step, an application of an insulative protection film, and a removal of part of that protection film, and since the "reasons provided above" do not mention any of those steps, the Examiner's basis for the rejection is unclear.

In regard to claim 8, it must be pointed out that the conductor pattern (which is formed so that a width of a bottom surface contacting the substrate is greater than a width of a top surface, which is opposite the bottom surface) is etched on an insulative substrate. Not only does the Kimiya reference fail to teach any such etching step, there isn't any such a conductor pattern on an insulative substrate disclosed in the Kimiya reference.

Regarding claim 8, it must be pointed out that the conductor pattern (which is formed so that a width of a bottom surface contacting the substrate is greater than a width of a top surface,

which is opposite the bottom surface) is etched on an insulative substrate. There isn't any such a conductor pattern on an insulative substrate disclosed in the Kimiya reference.

Based upon the present amendment and the comments above, Applicants respectfully request that the Examiner withdraw his rejection to claims 1 and 8.

Rejection of Claims Under 35 U.S.C. § 103

The Examiner rejected claims 1 through 9 under 35 U.S.C. §103(a), as being unpatentable over Dalal et al. (U.S. Patent number 5,634,268) in view of Nubuo et al. (Publication number 08181423). The Examiner stated:

> Note Fig. 6 of Dalal et al., where he/she shows a printed circuit board comprising: a substrate (10); a conductor pattern (20 and 18) formed on the substrate (see Fig. 6); and a protection film (22) coating the substrate and the conductor pattern (see Fig. 6), wherein the conductor pattern (20 and 18) includes a bottom surface contacting the substrate, a top surface opposite to the bottom surface, and a pair or side surfaces, each of the side surfaces having an upper side surface (20) exposed from the protection film, and the width or the bottom surface being greater than the width of the top surface (see Fig. 6) except a lower side surface (18) covered by the protection film. However, Nobuo et al. discloses a lower side surface covered by the protection film (see Fig. 9). Thus, it would have been obvious to one of ordinary in the skill in the art at the time when the invention was made to modify Dalal et al. by covering a lower side surface by the protection film as

taught by Nobuo et al. The ordinary artisan would have been motivated to modify Dalal et al. in the manner described above for at least the purpose of increasing protection for the conductor pattern.

Regarding claim 2, Dalal et al., as modified, disclose the conductor pattern (20 and 18) has a trapezoidal cross-section that is perpendicular to the longitudinal directional of the conductor pattern (See. Fig. 6).

Regarding claim 3, the phrase "the pair of side surfaces having concave surfaces" is structurally inherent in Dalal et al. in view of Nobuo et al.

Regarding claim 4, Dalal et al., as modified, discloses the height of the portion coated by the protection film (22) in the conductor pattern (20 and 18) is 50% or greater and less than 100% of the height of the conductor pattern.

Regarding claim 5, Dalal et al., as modified, discloses the top surface and the upper side surfaces being coated by a plate (43 and see Fig. 6).

Regarding claim 6, Dalal et al., as modified, discloses a solder ball (38) contacting the conductor pattern (20 and 18) at the upper side surfaces (See Fig. 6).

Regarding claim 7, Dalal et al., as modified, discloses a value obtained by dividing one half of a value obtained by subtracting the width of the top surface from the width of the bottom surface by the height of the conductor pattern is in the range of 0.1 to 2.5.

Regarding claim 8, the method steps are disclosed by Dalal et al. in view of Nobuo et al. for the same reasons provided above for the device claim 1.

Regarding claim 9, Dalal et al., as modified, discloses a fabrication method further comprising the steps of plating (43) the exposed upper portion (20) of the conductor pattern (20 and 18); and joining a solder ball (38) to the plated upper portion 920) of the conductor pattern (See. Fig. 6).

Reviewing Dalal et al., element 20 is identified as "a layer of copper" and element 18 is identified as "a very thin layer of chromium" used "to promote adhesion of the copper 20, to the laminate 10." While element 18 and 20 are both made of conductive materials, the element 18 is separate and distinct from the element 20, and the two elements have different uses. The very thin layer of chromium 18 is deposited on the upper surface 14 of the circuit card 25, and the copper is deposited on that very thin layer of chromium 18.

If the elements 18 and 20 are considered to act as a single conductive layer, then the embodiment shown in Fig. 6 of the Dalal et al. reference appears to be similar to the prior art shown in Fig. 6(A) of the present specification, except that the Dalal et al. embodiment lacks a protection film. This would make it less pertinent than the prior art already disclosed in the specification.

If the elements 18 and 20 are considered to act as two separate elements, then the Dalal et al. reference is given less pertinent, since it would be teaching the conductive pattern being laid on a conductor instead of being laid on the required insulative substrate.

The Examiner admits that a lower side surface covered by the protection film is not shown by Dalal et al., but he states that "Nobuo et al. discloses a lower side surface covered by the protection film (See Fig. 9)." Reviewing Fig. 9, it appears that the ENTIRE side surface of the conductive layer is covered. Specifically, Fig. 9 shows an electrode pad 2 on an insulative substrate 1, with ALL the side surface and part of the top surface of that electrode pad 2 being covered with an insulation film 3. The exposed part of the top of surface of the electrode pad 2, and part of the insulation film 3, is covered with a barrier metal 6, which is attached to a solder bump 4 by means of an adhesive layer 5. Clearly, Nobuo et al. fails to show what the Examiner thought that it did.

If the Dalal et al. reference were combined with the Nobuo et al., without the hindsight gained by reading the present specification, the results would be something similar to the problem shown in Fig. 7(A) of the specification. Since Nobuo et al. teaches completely coating the side surfaces, Dalal et al., as modified, would have the same problems of easy separation of the solder ball from the conductor pad when lateral force is applied.

Notice that both Dalal et al. and Nobuo et al. require the need of adhesive layers to maintain contact. Dalal et al. needs an adhesive layer 18 to keep the conductor pattern 20 attached to the circuit card, and Nobuo et al. needs an adhesive layer 5 to bind the barrier metal 6 with the solder bump 4. The invention of the present application achieves good adhesion because of the sufficient contact between the solder ball and the upper side surfaces.

Regarding claim 3, none of the figures of Dalal et al., or Nobuo et al. show side surfaces having concave surfaces. All of the side surfaces appear to be linear. There appears to be no teaching to use concave surfaces.

Regarding claim 4, Figure 6 of Dalal et al. clearly shows that the entire conductor pattern 20 is contacted with the eutectic 43. Only the very thin layer of chromium 18 is not so contacted. Therefore, even if someone were to modify the invention of Dalal et al., as suggested by the Examiner, to cover the "lower side surface (18)" with the protection film, the height of the portion coated by the protection film would be must less than 50%. My measurement from the drawing shows that the height would be, at the most, only about 23% of the height of the conductor pattern.

Regarding claim 8, the Applicants respectfully request that the Examiner clarify his comments. Since claim 8 is a method claim, with an etching step, an application of an insulative protection film, and a removal of part of that protection film, and since the "reasons provided above" do not mention any of those steps, the Examiner's basis for the rejection is unclear.

Based upon the present amendment and the comments above, Applicants respectfully request that the Examiner withdraw his rejection to claims 1 through 9.

For the above reasons, Applicants respectfully request that the Examiner withdraw his rejection and allow the case to issuance.

In view of the amendments and remarks presented above, the Applicants believe that the application is now in condition for allowance, and requests reconsideration of the application and

withdrawal of the objections and rejections. The Applicants respectfully request that the Examiner telephone the undersigned in the event a telephone conference would expedite prosecution of the application.

Respectfully submitted,

GODFREY & KAHN, S.C.

Dated: 2/7/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

In accordance with 37 C.F.R. § 1.121(b)(1)(ii), the following is a marked-up version of the replacement paragraphs of the specification.

The paragraph beginning at page 2, line 9, has been amended as follows:

To solve this problem, as shown in Fig. 6(A), the conductor patterns 93 may have a trapezoid cross-section in which the width a of the bottom surface 931 is greater than the width b of the top surface 932. However, in this case, the material forming the conductor patterns 93 forces the protection film 4 94, which is shaped in correspondence with the conductor patters 93, upward. Thus, as shown in Fig. 6(B), the protection film 94 may be separated from the upper surface of the substrate 2. Further, as shown in Fig. 6(C), during formation of the conductor patterns 93, a portion 939 of the conductor patterns 93 may enter the space between the bottom surface of the protection film 94 and the upper surface of the substrate 2 causing a short-circuit with the adjacent conductor pattern 93.

The paragraph beginning at page 13, line 20, has been amended as follows:

A second embodiment of a printed circuit board will now be discussed centering on the points differing from the first embodiment. As shown in Fig. 3, in the second embodiment, ~~the~~ an upper surface 42 of the solder resist 4 is shaped in correspondence with the arrangement of the conductor pattern 3. This is the only difference between the printed circuit boards of the second embodiment and the first embodiment.

The paragraph beginning at page 14, line 15, has been amended as follows:

A laser is irradiated against the upper surface ~~41~~ 42 of the solder resist 4 to remove the solder resist 4 along the conductor patterns 3, as shown in Fig. 4(C). Laser irradiation is stopped when 5% of the height p of the conductor pattern 3 is exposed. This exposes the upper portion 32 of the conductor pattern 3, or the top surface 320 and the side surfaces 325 to openings 40 of the solder resist 4. In this state, the height h of the lower portion 31 of the conductor pattern 3 is 95% of the height p of the conductor pattern 3.

In the Claims:

In accordance with 37 C.F.R. § 1.121(c)(1)(ii), the following is a marked-up version of the amended claims.

1. (Amended) A printed circuit board comprising:

~~a~~ an insulative substrate;

a conductor pattern formed on the substrate; and

a protection film coating the substrate and the conductor pattern, wherein the conductor pattern includes a bottom surface contacting the substrate, a top surface opposite to the bottom surface, and a pair of side surfaces, each of the side surfaces having a lower side surface covered by the protection film and an upper side surface exposed from the protection film, wherein both the bottom surface and the top surface have widths, both the lower side surface covered by the protection film and the conductor pattern have heights, and wherein the width of the bottom surface ~~being~~ is greater than the width of the top surface.

2. (Amended) The printed circuit board according to claim 1, wherein the conductor pattern has a trapezoidal cross-section that is perpendicular to the ~~longitudinal direction~~ bottom surface of the conductor pattern.

4. (Amended) The printed circuit board according to claim 1, wherein the height of the ~~portion coated~~ lower side surface covered by the protection film in the conductor pattern is 50% or greater and less than 100% of the height of the conductor pattern.

7. (Amended) The printed circuit board according to claim 1, wherein a value X is obtained by the following formula:

$X = ((c-d)/2)/p$

where c is the width of the bottom surface, d is the width of the top surface, and p is the height of the conductor pattern, and wherein X ~~dividing one half of a value obtained by subtracting the width of the top surface from the width of the bottom surface by the height of the conductor pattern~~ is in the range of 0.1 to 2.5.

8. (Amended) A method for fabricating a printed circuit board comprising the steps of:

etching ~~a~~ an insulative substrate including a conductor to form a conductor pattern, wherein the conductor pattern is formed so that a width of a bottom surface contacting the substrate is greater than a width of a top surface, which is opposite the bottom surface;

applying an insulative protection film to the conductor pattern and the substrate; and

removing part of the protection film to expose an upper portion of the conductor pattern.